EXHIBIT 1

To Defendant Dell Inc.'s Memorandum in Support of Its Motion to Compel Answers to Dell's Requests for Admission Nos. 27-57 to Plaintiff

"Defendant Dell Inc.'s First Set of Requests for Admission to Plaintiff"

Terry E. Welch (5819)
Darren K. Nelson (7946)
PARR WADDOUPS BROWN GEE & LOVELESS
185 S. State Street, Suite 1300
Salt Lake City, Utah
Telephone: 801-532-7840
Facsimile: 801-532-7750

Matthew M. Neumeier
Reginald J. Hill
Benjamin J. Bradford
JENNER & BLOCK LLP
One IBM Plaza
Chicago, IL 60611
Telephone: 312-222-9350
Facsimile: 312-527-0484

Attorneys for Dell Inc.

UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF UTAH CENTRAL DIVISION

PHILLIP M. ADAMS, and individual, and PHILLIP M. ADAMS & Associates, L.L.C., a Utah Limited Liability Company. Plaintiff. vs. DELL INC., FUJITSU LIMITED, FUJITSU COMPUTER SYSTEMS CORP., FUJITSU SIEMENS COMPUTERS GmbH, INTERNATIONAL BUSINESS MACHINES CORP., LENOVO INC., MPC COMPUTERS, LLC, SONY ELECTRONICS INC., Defendants.	**DEFENDANT DELL INC.'S FIRST SET OF REQUESTS FOR ADMISSION TO PLAINTIFF** Civil No. 1:05-CV-64 The Honorable Ted Stewart, Magistrate Judge David Nuffer

Defendant Dell Inc., ("DELL"), by its attorneys, hereby propounds the following Requests for Admission on Plaintiff Phillip M. Adams and Phillip M. Adams & Associates, L.L.C. ("Adams"), pursuant to Rule 36 of the Federal Rules of Civil Procedure.

DEFINITIONS

1. Adams means the Plaintiff Phillip M. Adams & Associates, L.L.C., Ltd. and any of its present or former affiliates, predecessors, successors, subsidiaries, assigns, employees, agents, representatives, directors or officers.

2. DELL means the Defendant Dell Inc. and any of its present or former affiliates, predecessors, successors, subsidiaries, assigns, employees, agents, representatives, directors or officers.

3. "Defendants" means DELL, Fujitsu Limited, Fujitsu Computer Systems Corp., International Business Machines Corp., Lenovo Group Ltd., MPC Computers, LLC, Sony Electronics Inc.

4. You, yours or your shall mean and refer to Phillip M. Adams & Associates, L.L.C..

5. The "'414 patent" means United States Patent No. 5,379,414.

6. The "'002 patent" means United States Patent No. 5,983,002.

7. The "'222 patent" means United States Patent No. 6,401,222.

8. "Patents-in-suit" means, collectively, individually or in any combination, the '414 patent, the '002 patent, or the '222 patent.

9. "FDC" means Floppy Diskette Controller and should be read consistent with the ordinary usage of the term in the computer industry.

10. For the purposes of these Requests for Admission, any term not specifically defined should be read consistent with the ordinary usage of the term in the computer industry. If Adams finds the meaning of any term in these requests for admissions to be unclear, Adams should assume a reasonable meaning consistent with its ordinary meaning in the art, state what the assumed meaning is, and answer the requests on the basis of that assumed meaning.

INSTRUCTIONS

1. Each response must consist of an answer or an objection to the particular request for admission.

2. Each answer must consist of one of the following: an admission, a denial, or a statement detailing why the answering party is unable to admit or deny.

3. If any portion of a request for admission is true, the responding party must admit that portion.

4. A denial of any or all of a request for admission must be specific.

5. These Requests for Admission seek responses as of the date of service hereof. However, pursuant to Rule 26(e) of the Federal Rules of Civil Procedure, these Requests for Admission shall be deemed continuing so as to require further and supplemental response by Adams in the event Adams or any person acting on its behalf obtains or discovers additional

information that may modify Adams's responses hereto, between the time of initial response and the time of hearing or trial as to the portion being denied.

6. Should you deem any information called for by any of the following Requests for Admission to be privileged and/or subject to the work product doctrine, specify the matter you claim to be privileged and/or subject to the work product doctrine and state all of the grounds and facts upon which such a claim rests, and on which you will rely to assert such a claim in order to provide the factual basis to determine whether such information is, in fact, privileged and/or subject to the work product doctrine.

7. These Requests for Admission are submitted for the purpose of determining the issues in dispute and are not to be taken as waiving any objections which may be made at trial to the introduction of evidence on subjects covered by the Requests for Admission or as an admission of the relevance or materiality at trial of any of the matters covered by these Requests for Admission.

REQUESTS FOR ADMISSION

Defendant DELL hereby requests that Plaintiff Adams admit the following:

1. ADMIT that as of June 15, 2006, Adams has not demonstrated to DELL that any of its computer models infringe the patents-in-suit.

2. ADMIT that as of June 15, 2006, Adams can identify by model name and number only one specific DELL computer model that Adams contends infringes the patents-in-suit.

3. ADMIT that as of June 15, 2006, Adams has not tested any DELL computers to determine if they have a faulty floppy disk controller.

4. ADMIT that as of June 15, 2006, Adams does not have a basis to believe that DELL ever possessed a copy of Adams's patented software.

5. ADMIT that as of June 15, 2006, Adams does not contend that Dell's computers infringe the patents-in-suit based on software running on the central processing unit that executes the operating system running on those computers.

6. ADMIT that as of June 15, 2006, Adams alleges that microcode contained in either a floppy disk controller or a super I/O device in a Dell computer infringes the patents-in-suit.

7. ADMIT that as of June 15, 2006, Adams has not tested the Dell Blade Server with product name Glacier to determine if it infringes the patents-in-suit.

8. ADMIT that as of June 15, 2006, Adams has not purchased the Dell Blade Server with product name Glacier.

9. ADMIT that as of June 15, 2006, Adams has never operated a Dell Blade Server with product name Glacier.

10. ADMIT that as of June 15, 2006, the Dell Blade Server with product name Glacier is the only specific Dell product that Adams alleges to infringe the patents-in-suit.

11. ADMIT that as of June 15, 2006, that the Winbond 83877 is the only Super I/O device found in a Dell product which Adams alleges infringes the patents-in-suit.

12. ADMIT that as of June 15, 2006, that the Winbond 83877 is the only Floppy Disk Controller found in a Dell product which Adams alleges infringes the patents-in-suit.

13. ADMIT that a floppy disk controller is required for direct infringement of the asserted claims of the patents-in-suit.

14. ADMIT that a floppy disk controller has to be operably connected a memory controller in order to directly infringe the asserted claims of the patents-in-suit.

15. ADMIT that a computer with only a floppy diskette drive that is connected to the computer via a universal serial bus cannot infringe the asserted claims of the patents-in-suit.

16. ADMIT that a floppy disk controller must be able to access a system clock in order to directly infringe the asserted claims of the patents-in-suit.

17. ADMIT that the presence of a floppy disk drive in a computer is not necessary for direct infringement of the asserted claims of the patents-in-suit.

18. ADMIT that a computer without a media drive cannot infringe the asserted claims of the patents-in-suit.

19. ADMIT that a computer without a media drive cannot infringe the asserted claims of the patents-in-suit.

20. ADMIT that a primary object of the '414 patent is to "provide a system and method for the detection … of an undetected FDC data error where data corruption occurs." at Col. 5, ll. 4-7.

21. ADMIT that a primary object of the '002 patent is to "provide a method for detecting defective Floppy Diskette Controllers ('FDCs')." at Col. 4, ll. 14-16.

22. ADMIT that a Floppy Diskette Controller is defective when it causes undetected data errors including data corruption.

23. ADMIT that a primary object of both the '414 and '002 patent is to provide a method for detecting defective Floppy Diskette Controllers.

24. ADMIT that a "prior solution" to the "FDC problem" is to "provide a new FDC that alleviates the problem." '414 patent, Col. 4, ll. 20-25.

25. ADMIT that at the time of the filing of the '414 patent a known solution to the "FDC problem" ('414 Patent, Col. 4, l. 20) was to use a new FDC which does not cause data corruption or data errors.

26. ADMIT that none of the patents-in-suit claim providing a new FDC to alleviate the FDC problem.

27. ADMIT that a "simple test program" to "demonstrate the FDC error" is disclosed in the '414 patent at Col. 2, l. 36 - Col. 3, l. 37.

28. ADMIT that the '414 patent discloses a "complete software implementation of a device driver that is capable of detecting an undetectable data corruption problem." Col. 19, ll. 36-39.

29. ADMIT that the element, "a processor executing detection executables effective to determine an underrun error undetected by a floppy diskette controller and effective to identify the floppy diskette controller as defective", contained in claim 1 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Perhaps the best way to

demonstrate the FDC error … has been demonstrated in systems using MS/PC-DOS operating systems by means of a simple test program" at Col. 2, ll. 36-42.

30. ADMIT that the element, "a memory device operably connected to the processor to store the detection executables and corresponding detection data", contained in claim 1 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "The architecture of a typical computer system is illustrated in FIG. 1. The computer system's CPU and main memory are located inside the system unit … to avoid losing the data, it must be saved on some type of storage device. For example, the computer system may use a 'hard disk' storage device which is permanently installed in the computer system." at Col. 6, ll. 20-32.

31. ADMIT that the element, "a system clock operably connected to the processor to provide a time base", contained in claim 1 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Virtually all computer systems must have a system clock" at Col. 6, ll. 61-62.

32. ADMIT that the element, "a media drive comprising storage media for storing data", contained in claim 1 of the '002 patent is disclosed by the '414 patent including, but not limited to, the descriptions "Most of these computer systems include diskette drives for storing and receiving data on floppy diskettes" at Col. 1, ll. 24-26 and "Most computer systems have at least one floppy diskette drive that receives a removable floppy diskette. That floppy diskette likewise is used for 'permanent' storage of data or software outside of the computer system" at Col. 6, ll. 32-36.

33. ADMIT that the element, "the floppy diskette controller operably connected to the media drive to control formatting and storage of data on the storage media", contained in

claim 1 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Data transfer to and from a floppy diskette is controlled by a ... Floppy Disk Controller" at Col. 1, ll. 36-37.

34. ADMIT that the element, "a direct memory access controller operably connected to the floppy diskette controller and the memory device to control transfers of data between the memory device and the floppy diskette controller", contained in claim 1 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "In transferring data to a floppy diskette, the CPU typically programs the Direct Memory Access (DMA) controller for an input/output ("I/O") transfer, issues a command to the FDC to begin the I/O transfer, and then waits for the FDC to interrupt with a completion interrupt signal. It is also possible to perform Programmed I/O ... without involving the DMA controller ... this latter approach is seldom used; the majority of computer systems employ DMA." at Col. 6, ll. 39-47.

35. ADMIT that the element, "The apparatus of claim 1 wherein the detection executables are effective to cause an underrun error", contained in claim 2 of the '002 patent is disclosed by the '414 patent including, but not limited to, the descriptions "Perhaps the best way to demonstrate the FDC error ... has been demonstrated in systems using MS/PC-DOS operating systems by means of a simple test program." at Col. 2, ll. 36-42 and "The results of using such a test program on various machines was quite astonishing. For example, the IBM PS/2 series seemed most susceptible to the problem, with roughly a 30% error rate." at Col. 2, ll. 52-56.

36. ADMIT that the element, "The apparatus of claim 2 wherein the detection executables cause the underrun error by delaying a transfer of data between the direct memory access controller and the floppy diskette controller", contained in claim 3 of the '002 patent is

disclosed by the '414 patent including, but not limited to, the description "One of the more simple examples is to begin a large transfer to the diskette and place that task in the background. After the transfer has begun then begin to display the contents of a very large file. The purpose of the video access is to force the video buffer memory refresh logic on DMA channel 1, along with the video memory access, to preempt the FDC operations occurring on DMA channel 2." at Col. 2, ll. 59-67.

37. ADMIT that the element, "The apparatus of claim 3 wherein the detection data comprises a test pattern", contained in claim 5 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred." at Col. 2, ll. 48-50.

38. ADMIT that the element, "The apparatus of claim 5 wherein the underrun error comprises the test pattern incorrectly copied onto the storage media", contained in claim 6 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred." at Col. 2, ll. 48-50.

39. ADMIT that the element, "The apparatus of claim 1 wherein the detection executables are integrated into an application directly loaded and executed on the processor", contained in claim 8 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "First, a clock program is executed and becomes a TSR (terminate and stay resident) task ... updating the time on the screen." at Col. 2, ll. 42-45.

40. ADMIT that dependent claim 10 of the '002 patent which states, "The apparatus of claim 1 wherein the detection executables include a shadowing executable effective to determine when a last byte is to be transferred from the direct memory access controller to the floppy diskette controller", is disclosed by the '414 patent including, but not limited to, the description "As used herein, DMA shadowing means monitoring byte transfers and then timing the last byte of a sector's DREQ to DACK signals. ... Once the byte counter has reached the last byte, the signal transition from DREQ to DACK is timed. If the time is greater than the time that will insure data integrity, an error condition is forced" at Col. 7, l. 43 - Col. 8, l. 15.

41. ADMIT that the element, "A memory device operably connected to a processor, a direct memory access controller, a floppy diskette controller controlled by the direct memory access controller, and a media drive controlled by the floppy diskette controller, the memory device storing blocks of data comprising:", contained in claim 11 of the '002 patent is disclosed by the '414 patent including, but not limited to, the descriptions:

a. "The architecture of a typical computer system is illustrated in FIG. 1. The computer system's CPU and main memory are located inside the system unit ... to avoid losing the data, it must be saved on some type of storage device. For example, the computer system may use a 'hard disk' storage device which is permanently installed in the computer system." at Col. 6, ll. 20-32;

b. "Most computer systems have at least one floppy diskette drive that receives a removable floppy diskette. That floppy diskette likewise is

used for 'permanent' storage of data or software outside of the computer system" at Col. 6, ll. 32-36;

c. "Data transfer to and from a floppy diskette is controlled by a … Floppy Diskette Controller" at Col. 1, ll. 36-37; and

d. "In transferring data to a floppy diskette, the CPU typically programs the Direct Memory Access (DMA) controller for an input/output ("I/O") transfer, issues a command to the FDC to begin the I/O transfer, and then waits for the FDC to interrupt with a completion interrupt signal. It is also possible to perform Programmed I/O ... without involving the DMA controller … this latter approach is seldom used; the majority of computer systems employ DMA." at Col. 6, ll. 39-47.

42. ADMIT that the element, "a test pattern", contained in claim 11 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred." at Col. 2, ll. 48-50.

43. ADMIT that the element, "detection executables effective to be run on the processor to force and detect an underrun error not detected by the floppy diskette controller", contained in claim 11 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred." at Col. 2, ll. 48-50.

44. ADMIT that the element, "a readback buffer to store a copy of the test pattern read back from the media drive", contained in claim 11 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred." at Col. 2, ll. 48-50.

45. ADMIT that the element, "writing a source test pattern from a memory device to storage media in a media drive controlled by the floppy diskette controller", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred." at Col. 2, ll. 48-50.

46. ADMIT that the element, "interrupting the writing step", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Importantly, concurrent execution is only 'simulated' because there is only one CPU, and it can only process one task at a time. Therefore, a system interrupt is used to rapidly switch between the multiple tasks" at Col. 2, ll. 12-17.

47. ADMIT that the element, "delaying a transfer of a last byte of the source test pattern to the floppy diskette controller to create the underrun error", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "__INT13_isr is responsible for receiving the INT 13 diskette interrupts from the O/S (BIOS). A check is made to see if the requested operation is a WRITE and the drive is a diskette (0 or 1). If so, then the timer is enabled and the system is set-up to delay the last (512th) byte of the transfer to generate an undetected underrun/overrun condition." at Col. 8, Remarks in Code Sample.

48. ADMIT that the element, "completing the writing step", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "The foregoing interposer routine checks to see if the request is a write operation. If so, then it calls .sub.- Timer.sub.- enable (reprogram the system clock), calls the original INT Ox13 Interrupt Service Routine (perform the actual write operation while DMA Shadowing is enabled), and finally calls .sub.-- Timer.sub.-- disable (reprograms the system clock to the original clock interrupt rate of approximately 54 milliseconds)." at Col. 9 ll. 23-30.

49. ADMIT that the element, "verifying whether the floppy diskette controller detected the underrun error", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "A running total of both detected and undetected errors can then be output to the display." at Col. 2 ll. 51-52.

50. ADMIT that the element, "The method of claim 12 further comprising reading back to the memory device a written test pattern corresponding to the source test pattern written during the writing step", contained in claim 13 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred" at Col. 2, ll. 48-50.

51. ADMIT that the element, "The method of claim 13 further comprising verifying whether the underrun error occurred in the writing step by checking the last byte of the written test pattern", contained in claim 14 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Once the sector has been written and read back the data is compared to determine whether or not an undetected error has occurred" at Col. 2, ll. 48-50.

52. ADMIT that the element, "a processor executing detection executables effective to precipitate and detect an underrun error undetected by a floppy diskette controller and effective to identify the floppy diskette controller as a defective floppy diskette controller", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Perhaps the best way to demonstrate the FDC error ... has been demonstrated in systems using MS/PC-DOS operating systems by means of a simple test program." at Col. 2 ll. 36-43.

53. ADMIT that the element, "a memory device operably connected to the processor to store the detection executables and corresponding detection data", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "The architecture of a typical computer system is illustrated in FIG. 1. The computer system's CPU and main memory are located inside the system unit ... to avoid losing the data, it must be saved on some type of storage device. For example, the computer system may use a 'hard disk' storage device which is permanently installed in the computer system." at Col. 6, ll. 20-32.

54. ADMIT that the element, "a system clock operably connected to the processor to provide a time base", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Virtually all computer systems must have a system clock." at Col. 6, ll. 61-62.

55. ADMIT that the element, "a media drive comprising storage media for storing data", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the descriptions "Most of these computer systems include diskette drives for storing and receiving data on floppy diskettes" at Col. 1, ll. 24-26 and "Most computer systems have at

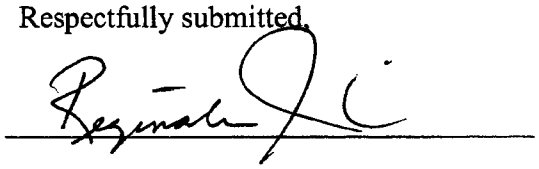
least one floppy diskette drive that receives a removable floppy diskette. That floppy diskette likewise is used for 'permanent' storage of data or software outside of the computer system" at Col. 6, ll. 32-36.

56. ADMIT that the element, "the floppy diskette controller operably connected to the media drive to control formatting and storage of data on the storage media", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "Data transfer to and from a floppy diskette is controlled by a ... Floppy Disk Controller" at Col. 1, ll. 36-37.

57. ADMIT that the element, "a direct memory access controller operably connected to the floppy diskette controller and the memory device to control transfers of data between the memory device and the floppy diskette controller.", contained in claim 12 of the '002 patent is disclosed by the '414 patent including, but not limited to, the description "In transferring data to a floppy diskette, the CPU typically programs the Direct Memory Access (DMA) controller for an input/output ("I/O") transfer, issues a command to the FDC to begin the I/O transfer, and then waits for the FDC to interrupt with a completion interrupt signal. It is also possible to perform Programmed I/O ... without involving the DMA controller ... this latter approach is seldom used; the majority of computer systems employ DMA." at Col. 6, ll. 39-47.

DATED: June 15, 2006

Respectfully submitted,



Reginald J. Hill
Matthew M. Neumeier
Benjamin J. Bradford
JENNER & BLOCK LLP
One IBM Plaza
Chicago, IL 60611
312 222-9350

Attorney for Dell Inc.